DIFFERENTIAL NON-VOLATILE CONTENT ADDRESSABLE MEMORY CELL AND ARRAY USING PHASE CHANGING RESISTOR STORAGE ELEMENTS

TECHNICAL FIELD

[0001] The present invention relates to a non-volatile differential content addressable memory cell using a phase changing resistor such as a chalcogenide storage element and an array. As a result memory cells in the same row do not require a word line to query the cells.

BACKGROUND OF THE INVENTION

[0002] Content addressable memory cells and arrays are well known in the art. U.S. Patent 5,949,696 discloses a differential volatile content addressable memory cell and an array made thereby.

[0003] Non-volatile content addressable memory cells and arrays are also well known in the art. U.S. Patent 5,930,161 discloses a non-volatile content addressable memory cell and array using ferroelectric capacitors as storage elements.

[0004] Non-volatile floating gate storage elements are also well known in the art. These can be of the stacked gate type or the split gate type as exemplified by U.S. Patent No. 5,029,130.

[0005] A differential non-volatile content addressable memory cell comprising a pair of non-volatile storage elements, and an array is also shown in U.S. Patent 6,639,818.

[0006] However, heretofore, all non-volatile differential content addressable memory cells and array have used a word line through the cells that are arranged in the same row to activate those cells.

[0007] Phase changing resistors, such as chalcogenide storage elements are also well known in the art.

[0008] It is therefore, an object of the present invention to provide a non-volatile differential content addressable memory without the use of word lines.

SUMMARY OF THE INVENTION

[0009] Accordingly, in the present invention, a content addressable memory cell comprises a first bit line for supplying a first bit. A first storage element has a first phase change resistor for storing a first stored bit, which is connected in series with a first diode. The first storage element is connected to the first bit line. A second bit line supplies a second bit, with the second bit being an inverse of the first bit. A second storage element has a second phase change resistor for storing a second stored bit, which is connected in series with a second diode. The second storage element is connected to the second bit line. A match line is connected to the first and second storage elements for indicating whether a match occurred between the first bit and the first stored bit, and between the second bit and the second stored bit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a schematic block level diagram of a differential non-volatile content addressable memory array of the present invention using the non-volatile content addressable memory cell of the present invention.

[0011] Figure 2A is a circuit diagram of a first embodiment of a differential non-volatile content addressable memory cell of the present invention which can be used in the array shown in Figure 1.

[0012] Figure 2B is a circuit diagram of a second embodiment of a differential non-volatile content addressable memory cell of the present invention which can be used in the array shown in Figure 1.

[0013] Figure 2C is a circuit diagram of a third embodiment of a differential non-volatile content addressable memory cell of the present invention which can be used in the array shown in Figure 1.

[0014] Figure 2D is a circuit diagram of a fourth embodiment of a differential non-volatile content addressable memory cell of the present invention which can be used in the array shown in Figure 1.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Referring to Figure 1, there is shown a schematic block level diagram of a differential non-volatile content addressable memory array 8 of the present invention. The array 8 comprises a plurality of non-volatile content addressable memory cells 10 arranged in a plurality of rows and columns. In Figure 1, the cells 10 are arranged in 4 rows by 4 columns. A match line ML (ML0...ML3) connects all the cells 10 in the same row and to an encoder 12. A pair of differential bit lines (BL0, BLN0...BL3, BLN3) connects all the cells 10 in the same column. The data to which a comparison to determine if a match exists is supplied to the reference word storage and bit line drivers 14. The data is then supplied to the particular column along a pair of particular bit lines. All the match lines (ML0...ML3) are connected to the encoder 12. When there is a match as determined by the particular match line going low (or high), the output of the encoder 12 indicates a hit as well as the address of the cell 10 where the match occurred.

[0016] Referring to Figure 2A there is shown a first embodiment of the non-volatile cell 10 that can be used in the array 8 of the present invention. The cell 10 comprises a first storage element 20a comprising of a first phase changing resistor, such as a chalcogenide resistor 22a connected in series with a first diode 30a. The first chalcogenide resistor 22a has a first end 24a and a second end 26a. The first diode 30a has an anode 32a and a cathode 34a. The anode 32a is connected to one of the bit lines, BL. The cathode 34a is connected to the first end 24a. The second end 26a is connected to the match line ML. The cell 10 also comprises a second storage element 20b comprising of a phase changing resistor, such as a second chalcogenide resistor 22b connected in series with a second diode 30b. The second chalcogenide resistor 22b has a first end 24b and a second end 26b. The second diode 30b has an anode 32b and a cathode 34b. The anode 32b is connected to the other of the bit lines, BLn. The cathode 34b is connected t o the first end 24b. The second end 26b is connected to the match line ML.

[0017] Referring to Figure 2B there is shown a second embodiment of the non-volatile cell 110 that can be used in the array 8 of the present invention. The cell 110 is identical to the cell 10

shown in Figure 2A except for the connection of the first diode 30a and the second diode 30b. In the second embodiment shown in Fig. 2B, the cathode 34a of the first diode 30a is connected to one of the bit lines, BL. The anode 32a is connected to the first end 24a of the first chalcogenide resistor 22a. The second end 26a is connected to the match line ML. Similarly, the cathode 34b of the second diode 30b is connected to the other of the bit lines, BLn. The anode 32b of the second diode 30b is connected to the first end 24b of the chalcogenide resistor 22b. The second end 26b of the second chalcogenide resistor 22b is connected to the match line ML.

[0018] Referring to Figure 2C there is shown a third embodiment of the non-volatile cell 210 that can be used in the array 8 of the present invention. The cell 210 is identical to the cell 10 shown in Figure 2A and the cell 110 shown in Figure 2B, except for the connection of the first diode 30a and the second diode 30b. In the third embodiment shown in Fig. 2C, the first end 24a of the first chalcogenide resistor 22a is connected to one of the bit lines, BL. The cathode 34a is connected to the second end 26a of the first chalcogenide resistor 22a. The anode 32a is connected to the match line ML. Similarly, the first end 24b of the second chalgogenide resistor 22b is connected to the other of the bit lines, BLn. The cathode 34b of the second diode 30b is connected t o the second end 26b of the second chalcogenide resistor 22b. The anode 32b of the second diode 30b is connected to the match line ML.

[0019] Referring to Figure 2D there is shown a fourth embodiment of the non-volatile cell 310 that can be used in the array 8 of the present invention. The cell 310 is identical to the cell 10 shown in Figure 2A, to the cell 110 shown in Figure 2B, and to the cell 310 shown in Figure 2C, except for the connection of the first diode 30a and the second diode 30b. In the fourth embodiment shown in Figure 2D, the first end 24a of the first chalcogenide resistor 22a is connected to one of the bit lines, BL. The anode 32a is connected to the second end 26a of the first chalcogenide resistor 22a. The cathode 34a is connected to the match line ML. Similarly, the first end 24b of the second chalcogenide resistor 22b is connected to the other of the bit lines, BLn. The anode 32b of the second diode 30b is connected to the second end 26b of the second chalcogenide resistor 22b. The cathode 34b of the second diode 30b is connected to the match line ML.

[0020] Each of the memory cells 10, 110, 210 or 310 can be used in the array 8 shown in Figure 1. To program or reset a cell 10, a first current (e.g. 0.2mA, if BL is to represent a bit of "1") is placed on the BL line. The BLn line is the inverse of the BL line. Thus, a second current, (e.g. 0.1mA, if 0.2mA is on BL) is placed on BLn. Of course, the current and the polarity may differ depending upon the memory cell 10, 110, 210 or 310 used. The match line ML is held at ground. Under this condition, first chalcogenide resistor 22a is programmed, when a current passes through the first chalcogenide resistor 22a, while second chalcogenide resistor 22b remains erased or set, since no current will flow. Once the first chalcogenide resistor 22a is programmed it will have a higher resistance than the second chalcogenide resistor 22b. The resistance of the first chalcogenide resistor 22a or the second chalcogenide resistor 22b "stores" the bit that is programmed therein. The unselected bit lines will all be held at the second current. Similarly, the cell 110 can be programmed by placing a first current, e.g. 0.2mA, on the match line. If BL has the bit "1", then it is held at the second current or 0.1mA, and BLn is held at the first current 0.2mA. First chalcogenide resistor 22a will then be programmed into a higher resistive state. The unselected bit lines will be held at the first current. The cell 210 can be programmed exactly like the cell 110, while the cell 310 can be programmed exactly like the cell 10.

[0021] Once the cell 10, 110, or 210, or 310 is programmed, the array 8 operates as follows. The reference word to be compared is first supplied to the reference word storage and bit line drivers 14. Let us assume that the reference word consists of four bits having a bit pattern of 1001. Assuming that the cell 10 is used in the array 8, the current supplied to the various bit lines is as follows:

BL0 – first current, e.g. 0.2mA, since the bit line is supplied with "1".
BLn0 – second current, e.g. 0.1mA, since the bit# line is supplied with "0"
BL1 – second current, e.g. 0.1mA, since the bit line is supplied with "0"
BLn1 – first current, e.g. 0.2mA, since the bit# line is supplied with "1"
BL2 – second current, e.g. 0.1mA, since the bit line is supplied with "0"
BLn2 – first current, e.g. 0.2mA, since the bit# line is supplied with "1"
BL3 – first current, e.g. 0.2mA, since the bit line is supplied with "1".
BLn3 – second current, e.g. 0.1mA, since the bit# line is supplied with "0"

[0022] From the foregoing it can be seen that if the chalcogenide resistors 22 of each cell 10 stores a resistance matching exactly as the bit pattern supplied on the bit lines, then little or no current would flow through any of the bit lines. For example, if the chalcogenide resistor 22 connected to bit line BL0 is programmed or reset to store "1", then it is at a high resistive value, and little or no current would therethrough to the match line. For the chalcogenide resistor 22 connected to BLn0, if it is erased or set, thereby storing a "0", the second current supplied to BLn0 would cause little or no current to flow therethrough. As a result, little or no current would flow through all of the bit lines to the match line ML. The testing of the match lines may be one at a time, or by the entire array 8. If the match lines of the array 8 are tested one by one, then the unselected match lines may be held at floating or at the first current (the diodes 30 in the cell 10 would prevent any current flowing from the unselected match line to the bit lines). After the testing of one match line, another match line would be selected for testing. Based upon the foregoing, if there is a mis-match, a current flow would be detected in the match line.

[0023] Because the array 8 does not use any word line, it is more compact. Thus, a more compact content addressable memory 8 using differential sensing non-volatile memory elements is provided. In addition, the array 8 is operated at a low operation voltage which is around Vcc, which is lower than the voltage of the non-volatile content addressable memories of the prior art.